noted that Chiang et al explicitly teach removing the oxide layer 4 from the top of the polysilicon line 3 (Fig. 5, Col. 4, lines 15-18). Applicant further disagrees that it would have been obvious to one having ordinary skill in the art at the time of the invention to include the liner oxide as taught by Ding et al in the teachings of Chiang et al to derive the device taught in Applicant's claimed invention.

Ding et al do show a dielectric layer 114 formed overlying the polysilicon layer 104a in Fig. 2H. However, Fig. 2H shows the device cross section across the channel from isolation 110 to isolation 110. Fig. 3 of Ding et al shows the cross section along the transistor ON current direction (or the direction that would show the source/drain regions in subsequent process steps). Fig. 3 of Ding et al corresponds, therefore, to the cross section depicted by the Applicant in Figs. 3 through 8. Note in Fig. 3 of Ding et al that the dielectric layer 114 (comprising, for example ONO), overlies the polysilicon layer 104b used for the floating gate by does not cover the sidewall of this gate 104b at the edges where source/drain regions would be formed.

More particularly, Ding et al teach in Column 4, lines 2-13: "The polysilicon layer 116 is patterned to form a control gate structure with a strip structure as can be seen in Fig. 1 with a shaded strip region, which is about vertically across the active area 109. The patterning process with same pattern mask is continuously performed to at least pattern the dielectric layer 114, the polysilicon spacer 112a, and the polysilicon layer 104a to expose the tunneling oxide layer 102a. The polysilicon layer 104a becomes polysilicon 104b. This patterning effect can be seen in another cross section view. Fig. 3 is a cross-sectional view of a portion of the substrate taken allon a line II-II in Fig. 1, schematically illustrating the structure of the flash memory, according to the preferred embodiment of the invention."

From the above citation, it is seen that Ding et al teach away from leaving this dielectric layer 114 covering the sidewalls of the polysilicon trace on the source/drain edges. By comparison, Applicant has amended Claim 17 to specifically teach the combined features of the liner oxide element, namely, that it overlies the polysilicon trace and that it covers the sidewalls of the trace at the edges where the source and drain

regions will be formed. The pertinent section of Amended Claim 17 is as follows:

17. (AMENDED) A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer;

a liner oxide layer overlying said polysilicon traces wherein said liner oxide layer covers sidewalls of said polysilicon traces on edges where source and drain regions are planned; . . .

Applicant submits that it is not obvious, for one skilled in the art at the time of the invention, to combine the teachings of Chiang et al and Ding et al to derive Applicant's Claimed invention, as recited in Amended Claim 17 for the following reasons: (1) While Chiang et al teaches an oxide layer on the polysilicon sidewalls, it teaches away from leaving this oxide layer overlying the polysilicon trace. (2) While Ding et al, shows a dielectric layer over the polysilicon trace, it teaches away from leaving the dielectric layer on the sidewalls of the polysilicon trace on the source/drain edges. (3) Applicant's Claimed invention teaches a liner oxide layer 60

feature that is present ***both*** overlying the polysilicon trace and covering the sidewalls of the source/drain edges. (4) Therefore, since Chiang et al and Ding et al each teach away from the combined features of the liner oxide layer in Applicant's claimed invention (overlying the polysilicon line ***and*** covering the sidewalls on the source/drain edge) then it is clear that Chaing et al and Ding et al, separately or in combination, cannot teach or suggest a way of forming a single liner oxide layer as taught by Applicant's Claimed invention such that one of ordinary skill in the art at the time of the invention could have made the invention.

Amended Claim 17 should not be found unpatentable over Chiang et al in view of Ding et al. In addition, Claim 21 has been amended to correct a typographical error. Amended Claim 21, as well as Claims 18-20, represent patentably distinct, further limitations on Amended Claim 17 and should also be in condition for allowance.

Reconsideration of Claims 17-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. Patent 6,235,600) in view of Ding et al (U.S. Patent 6,153,472) is

requested based on Amended Claims 17 and 21 on the above remarks.

Reconsideration of Claims 22-25 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. Patent 6,235,600) in view of Ding et al (U.S. Patent 6,153,472) and further in view of Chen et al (U.S. Patent 6,323,105) is requested based on Amended Claims 22 and 25 on the following remarks.

The above remarks concerning rejection of Claims 17-21 fully apply to the rejection of Claims 22-25. Claim 22 has been amended in similar fashion as Amended Claim 17. Chen et al do not teach or suggest a way of forming a single liner oxide layer as taught by Applicant's Claimed invention such that one of ordinary skill in the art at the time of the invention could have made the invention. Therefore, Chaing et al, Ding et al, and Chen et al, separately or in combination, cannot teach or suggest a way of forming a single liner oxide layer as taught by Applicant's Claimed invention such that one of ordinary skill in the art at the time of the invention could have made the invention. Claims 22-25 should be in condition for allowance.

Reconsideration of Claims 22-25 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. Patent 6,235,600) in view of Ding et al (U.S. Patent 6,153,472) and further in view of Chen et al (U.S. Patent 6,323,105) is requested based on Amended Claims 22 and 25 on the above remarks.

Reconsideration of Claims 26-28 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. Patent 6,235,600) in view of Ding et al (U.S. Patent 6,153,472) and further in view of Tsai (U.S. Patent 6,251,748) is requested based on Amended Claim 26 on the following remarks.

The above remarks concerning rejection of Claims 17-21 fully apply to the rejection of Claims 26-28. Claim 26 has been amended in similar fashion as Amended Claim 17. Tsai does not teach or suggest a way of forming a single liner oxide layer as taught by Applicant's Claimed invention such that one of ordinary skill in the art at the time of the invention could have made the invention. Therefore, Chaing et al, Ding et al, and Tsai, separately or in combination, cannot teach or suggest a way of forming a single liner oxide layer as taught by

Applicant's Claimed invention such that one of ordinary skill in the art at the time of the invention could have made the invention. Claims 26-28 should be in condition for allowance.

Reconsideration of Claims 26-28 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. Patent 6,235,600) in view of Ding et al (U.S. Patent 6,153,472) and further in view of Tsai (U.S. Patent 6,251,748) is requested based on Amended Claim 26 on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner F. Erdem not find that the Claims are now Allowable that he call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

Douglas R Schnabel

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please Amend Claim 17 as follows:

17. (AMENDED) A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer;

a liner oxide layer overlying said polysilicon traces wherein said liner oxide layer covers sidewalls of said polysilicon traces on edges where source and drain regions are planned;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped profile; and

an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.

Please Amend Claim 21 as follows:

21. (AMENDED) The [method] device according to Claim 17 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

Please Amend Claim 22 as follows:

22. (AMENDED) A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;

a liner oxide layer overlying said polysilicon traces wherein said liner oxide layer covers sidewalls of said polysilicon traces on edges where source and drain regions are planned;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped profile; and

an interlevel dielectric layer overlying said

polysilicon traces, said silicon nitride spacers, and said liner oxide layer.

Please Amend Claim 25 as follows:

25. (AMENDED) The [method] device according to Claim 22 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

Please Amend Claim 26 as follows:

26. (AMENDED) A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;

a liner oxide layer overlying said polysilicon traces wherein said liner oxide layer covers sidewalls of said polysilicon traces on edges where source and drain regions are planned;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped profile and wherein said silicon nitride layer is formed by chemical vapor deposition; and

an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.